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INVITED

Noise Spread Spectrum with Adjustable Notch Frequency in Complex Pulse Coding Controlled DC-DC Converters

Yasunori Kobori*, Nobukazu Tsukiji, Yifei Sun, Nobukazu Takai and Haruo Kobayashi

Gunma University, Japan

Outline

1. Background

- 1-1 Switching Converter
- 1-2 EMI Reduction with clock modulation

2. Pulse Coding and Notch Characteristics

- 2-1 Pulse coding control
- 2-2 Simulation result with PWC control
- 2-3 Experimental results of PWC control

3. Automatic PWC Control for Radio Receivers

- 3-1 Generating the clock using PLL circuit
- 3-2 Adjustable direct generation from input frequency

4. Conclusion

1. Background

Our Research about DC-DC converters



High Power Low ripple Fig.0 Our Research for Switching Converters

SIMO: Single-Inductor Multi-Output

Functions

Switching noise and EMI trouble



research process

- Reduce clock noise spectrum level below the Standard Level
- ▲ By shaking the clock phase/frequency, spread the clock noise around clock frequency and harmonics.
- Radio receivers would not like to be affected by spread noise.

X Our Objective

★ Develop Spread Spectrum Method both to reduce the EMI noise and



research process

- Reduce clock noise spectrum level below the Standard Level
- By shaking the clock phase/frequency, spread the clock noise around clock frequency and harmonics.
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X Our Objective

★ Develop Spread Spectrum Method both to reduce the EMI noise and to reject noise at desired frequency with Notch Characteristics.



1-1 Switching Converter (Buck type)

- * Output Voltage Vo is compared with Vref and amplified.
- * Amplified voltage \triangle Vo is compared with SAW-tooth signal. \Rightarrow Generate the Pulse Width Modulation (PWM) pulse.
- * Power SW is controlled by the PWM pulse.
- * Inductor Current changes Up/Down to control Vo stable.



Fig.1-2 Circuit of the Buck converter

- Spectrum of PWM pulse
- * Electro-Magnetic Interference (EMI) Noise [from Circuit]
- * Conductive Current Noise
- * Noise Spectrum (PWM pulse)
 - \Rightarrow High Level spectrum at Fck (=200 kHz) & harmonics.

[Input Current]

★ Reduce clock frequency spectrum



1-2 EMI reduction with clock modulation

* To reduce EMI noise, clock pulse is modulated.

 \Rightarrow Clock spectrum is spread and reduced.



Fig. 1-5 Converter with EMI reduction



Fig. 1-7 Digital EMI reduction

Fig.1-8 Timing chart 9

2) Linear sweep modulation:

* Clock pulse is generated using VCO.

- •VCO is modulated by Triangular signal with.
- * Spectrum of modulated PWM pulse
 - •Peak level is reduced and the top shape is flat.



(3) Random Analog noise modulation: * Pseudo Random Noise + PLL Circuit

- Random pattern is generated from M-sequence (3 bit) through LPF \Rightarrow pseudo random analog noise (Fig.1-12)
- Output of PLL circuit is the clock with random frequency.



 Simulated noise spectrum with EMI reduction Peak level is reduced to 2.0V (-4.9 dB) Harmonics are much reduced. (ex. -20 dB at 1.0 MHz) Output Voltage Ripple Vo is about 13 mVpp. (=0.3%)

Bottom levels increase high!

13mVpp



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2. Pulse Coding and Notch Characteristics

2-1 Pulse coding control

- ★ Switching Converter with Pulse Coding
- * Make SEL signal by comparing ⊿Vo vs. Vr
 • Select Pulse-H or Pulse-L.

Pulse-H: with H-Duty ratio

 In order to control Vo, duty ratios of coding pulses are very important.

★
$$D_H > D_O > D_L$$
 ··· (1)
Do= Vo∕Vin



Fig.2-1 Switching Converter with Pulse Coding

★ Pulse Coding control

- 1) Pulse Width Coding (PWC)
 - Pulse width is different.
 - Notch frequency: Fn

 $Fn = N/(W_H - W_L) \cdots (2)$

2) Pulse Phase Coding (PPC)
Pulse phase is different.
Fn = N/(2 · 7) · · · · (3)



3) Pulse Cycle Coding (PCC)

• Pulse cycle (period) is different.

$$Fn = N/(T_L - T_S) \cdots (4)$$

★ Complex Pulse Coding control

1) Pulse Width & Phase Coding (PWPC)

- Pulse width & phase are different.
- Notch frequency: Fn

 $Fn1 = N/(2 \cdot \tau)$ Fn2 = M/(T_L-T_S)

2) Double notch characteristics When set $\tau = (T_L - T_S)/2 \cdots$ (5) then Fn1 = Fn2. : Double Notch



2-2 Simulation result with PWC control





Fig.2-4 PWC Pulses



- Noise Spectrum with PWC control of PWM pulse
- * Notch Freq. : $F_N = N/(W_H W_L) = N/1.3us = 0.77$, 1.5 MHz Peak Level Reduction: $3.5V \Rightarrow 0.9V (-11.8 \text{ dB})$
- * Frequency relation : Fck < Fn < 2Fck



Fig. 2-7 Noise Spread Spectrum with PWC control

Noise Spectrum with PWPC control:

* Conditions: Vi=10V, Vo=5.0V, Fck=1.4 MHz (Tck=714 ns)

 $W_{H} = 480 \text{ ns}, W_{L} = 320 \text{ ns}, \tau = (W_{H} - W_{L})/2 = 80 \text{ ns}$

* Notch Frequency: $F_N = 1/160ns = 6.25 MHz$

Bottom Level: $V_B: -65dB \Rightarrow -75 dB (-10dB)$



2-3 Experimental result with PWC control

* Conditions : W_H =5.0 ns, W_L =1.0 ns, Tck=160 kHz * Notch Frequency: Fn=1/(5.0-1.0) us = 250 kHz * Relation: Fck < Fn=274 kHz < 2 · Fck



Fig.2-9 Noise spectrum & major signals with PWC

Experimental result 2 with PWC

- * Conditions 2: W_H = 2.0 ns, W_L = 1.0 ns, Fck=420 kHz
- * Notch Freq.: $F_N = 1 / (2.0 1.0) us = 1.0 MHz$
- * Relation: $2 \cdot \text{Fck} < \text{Fn} = 1.05 \text{ MHz} < 3 \cdot \text{Fck}$





Fig. 2-10 Another noise spectrum with PWC 2

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3. Automatic PWC Control for Radio Receiver

3-1 Generating clock pulse & coding pulses

- Relations among Fin, Fck, Fn and W_H, W_L
- * Better to generate Fn at middle of Fck :
 - N=1: Fck < Fn $< 2 \cdot$ Fck
 - •N=2: 2 · Fck < Fn < 3 · Fck
 - $\therefore Fn = (N+0.5) \cdot Fck \Rightarrow Tck=Tn \cdot (N+0.5) \qquad \cdots (7)$

* Static duty ratio Do and Coding pulses

- Do = Vo / Vin, $Tn = W_H W_L = Tin$...(8)
- $W_H = Do \cdot Tck + Tin/2$, $W_L = Do \cdot Tck Tin/2$...(9)

★ After generating Tck from Tin, $W_H \& W_L$ are set with Eq. (9). ★ Case: N=1, Do=0.5

 $Tck = Tin \cdot (N+0.5) = 1.5 \cdot Tin \implies 2 \cdot Tck = 3 \cdot Tin \cdots (10)$

How to generate Fck from Fin
 (A) using PLL circuit
 (B) Using Direct calculation

(A) Generating Tck using PLL circuit : (Presentation IPS01-03 [Sun])

* Use VCO and generate $Fck = (2/3) \cdot Fin$

* Generate coding pulses W_H , W_L from Tin & Tck

 $W_{H} = Tin/2 + Tck/2, W_{L} = Tin/2 - Tck/2 \qquad \cdots (9')$

Fin P.C Fck 1/3 \times vco \rightarrow 1/3 1/3 1/2 1/2

P.C : Phase Comparator VCO: Voltage Controlled Oscillator

Fig. 3-1 PLL circuit with VCO



Fig. 3-2 Generating W_H & W_L 24

- * Simulation result: Fin =500 kHz
 - Noise spectrum: Fck= 330 kHz, Fn=520 kHz
 - Step Response with Fin change: @ Fin=0.5MHz ⇔ 1.0MHz Ripple=15mVpp, Undershoot=-15mV
 Settling time (recovery time): Ts = 0.15 ms



(B) Generating Tck using Direct calculation

- * Generate Tck from Tin using Eq. 10 : Tck = 1.5 · Tin (N=1)
 Measure Tin and generate Tck using digital/analog circuit.
- * Calculate coding pulses $W_H \& W_L$ from Tin & Tck $W_H = Tin/2 + Tck/2, W_L = Tin/2 - Tck/2 \cdots$ (9')
- Simulation result: Fin=750 kHz
 - Static voltage ripple: ∠Vo = 3mV @ Fin= 750kHz
 - Step Response: when Fin = 1.25M ⇔ 1.0M ⇔ 0.75MHz
 ∠Vo = Over/Undershoot = 4mV, Settling time ≒ 0 ms



- Noise spectrum with Linier sweep EMI reduction
- * Case 1: Fin= 750 kHz, N=1
 - Fn=750 kHz, Fck=500 kHz, Fck < Fn < 2Fck
- * Case 2: Fin=1.25 MHz, N=2
 - Fn=1.27 MHz, Fck=500 kHz, 2Fck < Fn < 3Fck
- There appears the large notch at 4.Fn



Conclusion

- ★ Developed Pulse Coding Control in order to generate notch characteristics at desired frequency.
- 1. Theoretical Notch Frequency:
 - **PWC** : $F_N = N \swarrow (W_H W_L)$
 - **PPC** : $F_N = N \swarrow (2\tau)$
 - PCC : $F_N = N \swarrow (T_L \frown T_S)$

* Complex Pulse Coding PWPC=PWC+PPC

- 2. Experimental Noise Spectrum with PWC :
 - Notch appears at Fn = (N+0.5) · Fck
- 3. Automatic notch generating method:
 - Generate Fck from Fin : Fck=2/3 · Fin (or Tck=1.5 · Tin) (A) using PLL circuit (B) using Direct Calculation
 Make W_H & W_L from Tin & Tck and set Fn:
 - \Rightarrow W_H=Tin/2+Tck/2, W_L=Tin/2-Tck/2
- Future Work:

Investigate why the large notch at 4. Fn appear.

Thank you for your kind attention!

Is there any question?